A Silicon Receiver for 100 Gb/s PDM-DQPSK Signals

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Abstract: We demonstrate a monolithically-integrated silicon photonic receiver for 100 Gb/s PDM-DQPSK signals. The device is realized with a 2D grating coupler, four Mach-Zehnder delay interferometers with phase shifters and four germanium balanced photodetectors.

I. INTRODUCTION

Compact silicon devices working at high speed with low power consumption are expected to foster the deployment of broadband optical interconnections in different segments of the global communication network. In this framework, the development of high-speed silicon transceivers capable of generating and receiving multilevel modulation formats is critical. For short-reach and interconnection links the use of differential decoding without coherent detection and digital signal processing techniques would simplify transceiver architecture and reduce energy consumption. Differential quadrature phase-shift keying (DQPSK) signals can be received using a pair of Mach-Zehnder delay interferometers (DIs), while polarization division multiplexed (PDM)-DQPSK signals require two of these circuits in parallel. Recently, a 43 Gb/s (10.7 Gbaud) PDM-DQPSK silicon receiver with endless polarization controllers has been reported [1]. Single polarization receivers using either hybrid integration [2] or flip-chip bonded photodetectors [3] have been also reported. In this paper we demonstrate a monolithically integrated silicon receiver consisting of a 2D grating coupler, four Mach-Zehnder delay interferometers with phase shifters and four germanium (Ge) balanced photodetectors. We demonstrate operation up to 25 Gbaud. The device can be used as a single polarization 50 Gb/s receiver in polarization diversity configuration or as a 100 Gb/s receiver for PDM signals. This is, to the best of our knowledge, the highest speed non-coherent monolithically-integrated silicon photonic receiver demonstration reported.

II. DEVICE DESIGN AND CHARACTERIZATION

A photograph and the mask layout of the fabricated photonic integrated circuit (PIC) are shown in Fig. 1. A 2D normal incidence surface grating coupler separates the light into four waveguides; two with X polarization and two with the orthogonal Y polarization, while also performing polarization rotation so that all light on the chip is TE polarized [4]. One X and one Y portion are coupled to two identical DQPSK receivers. The other X and Y portions are coupled to integrated Ge photodetectors for polarization monitoring and for characterizing the extinction ratio (ER) between the two orthogonal signals. Fig. 2 reports the measured ER between the two monitored 2D grating output ports. The input state of polarization is adjusted with a polarization controller (PC) in order to maximize the output power at the X or Y port. Photocurrent is measured from the monitor photodetectors. The resulting ER over the C-band is measured to be in the range of 15-24 dB and 11-21 dB for the two grating outputs respectively.

The receiver consists of two directional couplers, two DIs, two balanced Ge photodetectors and the two single Ge photodetectors for polarization monitoring. The differential delay for the DIs is designed to be 40 ps, which corresponds to a baud rate of 25 Gbaud. Both strip and rib waveguides are utilized to optimize footprint while maintaining low optical losses. The two waveguides are combined in a 2x2 directional coupler. The DIs of the DQPSK receiver convert the differential phase modulation to intensity modulation for each signal carrier that is received by the balanced photodetectors.
The PIC was fabricated at the Institute of Microelectronics (IME), Singapore, through the OpSIS (Optoelectronic Systems Integration in Silicon) foundry [5] on 220 nm silicon on insulator (SOI) wafers where the buried oxide is 2 μm thick. Strip waveguides are typically 500 nm wide and the minimum bending radius used for designing the receiver is 5 μm. The DI includes two thermal phase shifters (one in each branch). The thermal phase shifters are realized with resistive heaters and the total phase shifter length is 500 μm. The DI length is 3.24 mm and the calculated TE mode group index is 3.69. Figure 3 shows the spectral response of the DI for two different voltages applied to the phase shifter. The same behavior is verified for each of the receiver DI. The measured frequency is 23 GHz corresponding to a delay of 43.4 ps. The ER is greater than 10 dB. Ge is deposited on the silicon waveguides for photodetection. Two Ge photodetectors are connected in series to form balanced photodetectors. On-chip capacitors are also integrated for DC decoupling. Typical responsivity, dark current and photodetectors are connected in series to form balanced photodetectors. On-chip capacitors are also integrated for DC decoupling. Typical responsivity, dark current and bandwidth of single photodetectors are 0.55 A/W, 5 μA (at 4 V reverse bias) and 20 GHz respectively [5].

III. RECEIVER MEASUREMENT RESULTS

As shown in Fig. 4, a variable symbol rate DQPSK signal is generated using a transmitter with a DFB laser operating at 1548 nm modulated by a nested Mach-Zehnder I-Q modulator driven by a 2'-1 pseudo random binary sequence (PRBS). The signal is amplified with an erbium doped fiber amplifier (EDFA) and is then combined with a filtered amplified spontaneous emission (ASE) source in order to vary the optical signal to noise ratio (OSNR).

The signal is polarization controlled before coupling to the PIC through the grating coupler. Polarization independent coupling is possible through the 2D coupler, or a single polarization grating coupler can be used for illuminating the two pairs of DI. The RF signals are collected from the balanced photodetectors through a probe array and are then amplified with low noise electrical amplifiers before analysis. The signals can be analyzed alternatively by a sampling oscilloscope or by an error analyzer for bit error rate (BER) measurements. Figure 5 shows the measured BER vs. OSNR for two different symbol rates, 20 and 25 GBaud, and for the two parallel DQPSK receivers varying the input polarization. The input optical power is 9 dBm. As shown in Fig. 5, the receiver sensitivity is 35 dB OSNR at 20 GBaud (with the exception of one poorly performing branch), even if there is a BER floor that is most likely due to the electrical noise of the measurement equipment. There is instead a BER floor near $10^{-3}$, which is, however, well below the FEC limit, for 25 GBaud signals. This is due primarily to limited photodetector bandwidth and small inaccuracy of the DI length. Example eye diagrams for the two quadratures are also shown in Fig. 5.

IV. CONCLUSIONS

A novel monolithically-integrated non-coherent silicon photonic receiver for PDM-DQPSK signals has been designed and fabricated. BER measurements show that the receiver can work largely under the FEC limit for 25 GBaud signals up to 100 Gb/s.

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